Experiment 20 – Quadrature Phase Shift Keying

Preliminary discussion
As its name implies, quadrature phase shift keying (QPSK) is a variation of binary phase shift keying (BPSK). Recall that BPSK is basically a DSBSC modulation scheme with digital information for the message. Importantly though, the digital information is sent one bit at a time. QPSK is a DSBSC modulation scheme also but it sends two bits of digital information at a time (without the use of another carrier frequency).

As QPSK sends two bits of data at a time, it's tempting to think that QPSK is twice as fast as BPSK but this is not so. Converting the digital data from a series of individual bits to a series of bit-pairs necessarily halves the data's bit-rate. This cancels the speed advantage of sending two bits at a time.

So why bother with QPSK? Well, halving the data bit rate does have one significant advantage. The amount of the radio-frequency spectrum required to transmit QPSK reliably is half that required for BPSK signals. This in turn makes room for more users on the channel.

Figure 1 below shows the block diagram of the mathematical implementation of QPSK.
At the input to the modulator, the digital data's even bits (that is, bits 0, 2, 4 and so on) are stripped from the data stream by a "bit-splitter" and are multiplied with a carrier to generate a BPSK signal (called PSK₁). At the same time, the data's odd bits (that is, bits 1, 3, 5 and so on) are stripped from the data stream and are multiplied with the same carrier to generate a second BPSK signal (called PSK₂). However, the PSK₂ signal's carrier is phase-shifted by 90° before being modulated. This is the secret to QPSK operation.

The two BPSK signals are then simply added together for transmission and, as they have the same carrier frequency, they occupy the same portion of the radio-frequency spectrum. While this suggests that the two sets of signals would be irretrievably mixed, the required 90° of phase separation between the carriers allows the sidebands to be separated by the receiver using phase discrimination (introduced in Experiment 8).

Figure 2 below shows the block diagram of the mathematical implementation of QPSK demodulation.

Notice the arrangement uses two product detectors to simultaneously demodulate the two BPSK signals. This simultaneously recovers the pairs of bits in the original data. The two signals are cleaned-up using a comparator or some other signal conditioner then the bits are put back in order using a 2-bit parallel-to-serial converter.
To understand how each detector picks out only one of the BPSK signals and not both of them, recall that the product detection of DSBSC signals is “phase sensitive”. That is, recovery of the message is optimal if the transmitted and local carriers are in phase with each other. But the recovered message is attenuated if the two carriers are not exactly in phase. Importantly, if the phase error is 90º the amplitude of the recovered message is zero. In other words, the message is completely rejected (this issue is discussed in Part E of Experiment 9).

The QPSK demodulator takes advantage of this fact. Notice that the product detectors in Figure 2 share the carrier but one of them is phase shifted 90º. That being the case, once the phase of the local carrier for one of the product detectors matches the phase of the transmission carrier for one of the BPSK signals, there is automatically a 90º phase error between that detector’s local carrier and the transmission carrier of the other BPSK signal. So, the detector recovers the data on the BPSK signal that it’s matched to and rejects the other BPSK signal.

The experiment
In this experiment you’ll use the Emona DATEx to generate a QPSK signal by implementing the mathematical model of QPSK. Once generated, you’ll examine the QPSK signal using the scope. Then, you’ll examine how phase discrimination using a product detector can be used to pick-out the data on one BPSK signal or the other.

It should take you about 1 hour to complete this experiment.

Equipment

- Personal computer with appropriate software installed
- NI ELVIS plus connecting leads
- NI Data Acquisition unit such as the USB-6251 (or a 20MHz dual channel oscilloscope)
- Emona DATEx experimental add-in module
- two BNC to 2mm banana-plug leads
- assorted 2mm banana-plug patch leads
Procedure

Part A - Generating a QPSK signal

1. Ensure that the NI ELVIS power switch at the back of the unit is off.

2. Carefully plug the Emona DATEx experimental add-in module into the NI ELVIS.

3. Set the Control Mode switch on the DATEx module (top right corner) to PC Control.

4. Check that the NI Data Acquisition unit is turned off.

5. Connect the NI ELVIS to the NI Data Acquisition unit (DAQ) and connect that to the personal computer (PC).

6. Turn on the NI ELVIS power switch at the back then turn on its Prototyping Board Power switch at the front.

7. Turn on the PC and let it boot-up.

8. Once the boot process is complete, turn on the DAQ then look or listen for the indication that the PC recognises it.

9. Launch the NI ELVIS software.

10. Launch the DATEx soft front-panel (SFP) and check that you have soft control over the DATEx board.
11. _Connect the set-up shown in Figure 3 below._

**Note:** Insert the black plugs of the oscilloscope leads into a ground (GND) socket.

![Figure 3](image)

The set-up in Figure 3 can be represented by the block diagram in Figure 4 below. The Sequence Generator module is used to model digital data. The 2-bit Serial-to-Parallel Converter module is used to split the data bits up into a stream of even bit and odd bits.

![Figure 4](image)
12. Set up the scope per the procedure in Experiment 1 with the following change:

- Trigger Source control to TRIGGER instead of CH A

13. Activate the scope’s Channel B input to observe the Serial-to-Parallel Converter module’s two outputs.

14. Compare the signals. You should see two digital signals that are different to each other.

**Question 1**
What is the relationship between the bit rate of these two digital signals and the bit rate of the Sequence Generator module’s output? **Tip:** If you’re not sure, see the preliminary discussion.

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Ask the instructor to check your work before continuing.

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15. Modify the set-up as shown in Figure 5 below.

**Remember:** Dotted lines show leads already in place.
Excluding the digital data modelling, the set-up in Figure 5 can be represented by the block diagram in Figure 6 below. Notice that the bit-splitter's two outputs are connected to independent Multiplier modules. The other input to the Multiplier modules is a 100kHz sinewave. However, the signals are out of phase with each other by 90° which is a requirement of QPSK.

16. Set the scope's Timebase control to the 200μs/div position.

17. Compare the even bits of data with the Multiplier module's output (PSK\(_I\)).

   **Tip:** You may find this easier to do if you set the scope’s Channel B Scale control to the 2V/div position.

18. Set the scope's Trigger Source control to the CH A position.

19. Set the scope's Timebase control to the 50μs/div position.

20. Examine the carrier and look closely at the way it changes at the sequence's transitions.
Question 2
What feature of the Multiplier's output suggests that it's a BPSK signal?

Ask the instructor to check your work before continuing.

21. Return the scope's Timebase control to the 500µs/div position and the Trigger Source to the Trigger position.

22. Move the scope's connections as shown in Figure 7 below.

Figure 7

This change can be shown on the block diagram in Figure 8 on the next page.
23. Set the scope’s Timebase control to the 200µs/div position.

24. Compare the even bits of data with the Multiplier module’s output (PSK₁).

25. Set the scope’s Trigger Source control to the CH A position.

26. Set the scope’s Timebase control to the 50µs/div position.

27. Examine the carrier and look closely at the way it changes at the sequence’s transition.

**Question 3**
What type of signal is present on the Multiplier’s output?
28. Return the scope's Timebase control to the 500µs/div position and the Trigger Source to the Trigger position.

29. Modify the set-up as shown in Figure 9 below.

![Figure 9](image)

This set-up can be represented by the block diagram in Figure 10 on the next page. The Adder module is used to add the PSK_I and PSK_Q signals. This turns the set-up into a complete QPSK modulator.

Ask the instructor to check your work before continuing.
30. Disconnect the patch lead to the Adder module’s $A$ input.

**Note:** This removes the $\text{BPSK}_I$ signal from the signal on the Adder module’s output.

31. Locate the Adder module on the DATEx SFP and adjust its soft $g$ control to obtain a 4Vp-p output.

32. Reconnect the patch lead to the Adder module’s $A$ input.

33. Disconnect the patch lead to the Adder module’s $B$ input.

**Note:** This removes the $\text{BPSK}_Q$ signal from the signal on the Adder module’s output.

34. Adjust the Adder module’s soft $g$ control to obtain a 4Vp-p output.

35. Reconnect the patch lead to the Adder module’s $B$ input.

**Question 4**

According to the theory, what type of digital signal transmission is now present on the Adder’s output?
QPSK or OQPSK: What’s the difference?

QPSK modulation is normally generated from a single data stream converted to two parallel data streams. In this particular experiment, the serial/parallel converter outputs the parallel streams such that the bits are offset from each other by one clock period. Therefore, in this experiment we are actually implementing a form of QPSK known as Offset QPSK (OQPSK).

Ask the instructor to check your work before continuing.
Part B – Observations of QPSK bandwidth in the frequency domain

One of the advantages of QPSK over BPSK is its higher data rate for the same bandwidth. The next part of the experiment lets you see this for yourself using the NI ELVIS Dynamic Signal Analyzer.

36. Disconnect the patch lead to the Adder module’s A input.

   Note: This removes the BPSK signal from the signal on the Adder module’s output, effectively turning the signal into simple BPSK.

37. Suspend the scope VI’s operation by pressing its RUN control (bottom left of VI window) once.

   Note: This should freeze the display.

38. Launch the NI ELVIS Dynamic Signal Analyzer VI.

39. Adjust the Signal Analyzer’s controls as follows:

   General
   Sampling to Run

   Input Settings
   ▪ Source Channel to Scope CHB
   ▪ Voltage Range to ±10V

   FFT Settings
   ▪ Frequency Span to 200,000
   ▪ Resolution to 400
   ▪ Window to 7 Term B-Harris

   Averaging
   ▪ Mode to RMS
   ▪ Weighting to Exponential
   ▪ # of Averages to 3

   Triggering
   ▪ Triggering to Scope Trigger

   Frequency Display
   ▪ Units to dB
   ▪ RMS/Peak to RMS
   ▪ Scale to Auto
   ▪ Markers to OFF
40. Reconnect the patch lead to the Adder module's A input while watching the Signal Analyzer's display carefully.

**Note:** Doing this turns the system back into a QPSK modulator and so doubles the data rate.

**Question 5**
What effect did doubling the data rate have on the signal's bandwidth?

**Question 6**
Did adding the BPSK signal have any effect on the Adder module's output? If so, what?

Ask the instructor to check your work before continuing.
Part C – Using phase discrimination to pick-out one of the QPSK signal’s BPSK signals

It’s not possible to implement both a QPSK modulator and a full demodulator with just one Emona DATEx module. However, it is possible to demonstrate how phase discrimination is used by a QPSK demodulator to pick-out one or other of the two BPSK signals that make up the QPSK signal. The next part of the experiment lets you do this.

41. Close the NI ELVIS Dynamic Signal Analyzer VI.

42. Locate the Phase Shifter module on the DATEx SFP and set its soft *Phase Change* control to the 0° position.

43. Modify the set-up as shown in Figure 11 below.

*Note:* As there are a lot of connections, you may find it helpful to tick them off as you add them.

![Figure 11](image)

The additions to this set-up can be represented by the block diagram in Figure 12 on the next page. If you compare the block diagram to Figure 2 in the preliminary discussion, you’ll notice that it implements most of one arm of a QPSK demodulator (either I or Q).
44. Restart the scope’s VI by pressing its RUN control once.

45. Compare the even data bits on the Serial-to-Parallel Converter module’s X1 output with the data on the output of the Baseband LPF.

46. Vary the Phase Shifter module’s soft Phase Adjust control left and right and observe the effect on the demodulated signal.

47. Set the Phase Shifter module’s soft Phase Change control to the 180° position and repeat step 46.

**Question 7**
The distortion makes it difficult if not impossible to tell when the even data bits have been recovered. What is needed to clean-up the recovered digital data?

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Ask the instructor to check your work before continuing.
48. Modify the set-up as shown in Figure 13 below.

![Figure 13](image)

The addition of the Comparator on the Utilities module can be represented by the block diagram in Figure 14 on the next page. If you compare this block diagram with Figure 2 in the preliminary discussion, you'll notice that this change completes one arm of a QPSK demodulator.
49. Return the Phase Shifter module’s soft *Phase Change* control to the 0° position.

50. Compare the even data bits on the Serial-to-Parallel Converter module’s X1 output with the data on the output of the Baseband LPF.

51. Adjust the Phase Shifter module’s soft *Phase Adjust* control until you have recovered the even data bits (ignoring any phase shift).

**Question 8**
What is the present phase relationship between the local carrier and the carrier signals used to generate the PSK₁ and PSK₂ signals?

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Ask the instructor to check your work before continuing.
52. Unplug the scope’s Channel A input from the Serial-to-Parallel Converter module’s $X1$ output and connect it to its $X2$ output to view the odd data bits.

53. Compare the odd data bits with the recovered data. They should be different.

54. Set the Phase Shifter module’s soft $Phase$ $Change$ control to the $180^\circ$ position.

55. Adjust the Phase Shifter module’s soft $Phase$ $Adjust$ control until you have recovered the odd data bits (ignoring any phase shift).

**Question 9**
What is the new phase relationship between the local carrier and the carrier signals used to generate the PSK$_1$ and PSK$_2$ signals?

**Question 10**
Why is your demodulator considered to be only one half of a full QPSK receiver?

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Ask the instructor to check your work before finishing.